

FET APPLICATIONS:

The bipolar transistor is the backbone of electronics. For certain applications, however, the FET is preferred. FET is the abbreviation used for these devices and stands for field effect transistor. How this name was derived will be explored during this lesson. FET's have numerous applications, including controlled switching from a conducting to a nonconducting state. This feature is useful in digital circuits. FET's are very suitable for integration on a single chip, as many thousands of FET's are commonly used together in semiconductor memory devices.

THE MAIN ADVANTAGES OF FET's:

High input impedance is the primary advantage of the FET. This quality enables an input signal to be close to zero power, yet still produce an output signal. The high input impedance also produces less loading which adversely affects the gain of a transistor. There is, however, a price to pay for this advantage. This large input resistance causes the FET to be less sensitive to input voltage changes than its bipolar counterpart. This results in a smaller possible voltage gain than is produced by the bipolar transistor.

Six additional advantages can be obtained when the FET is used

1. Operates at low DC voltages.
2. The device is light in weight.
3. It is small in size.
4. It is mechanically rugged.
5. It operates without generating much heat.
6. The FET will produce less noise than a bipolar device (low noise figure).

BIPOLAR AND UNIPOLAR DEVICES; A COMPARISON:

The transistors discussed in previous lessons have all been bipolar. This means that both electrons and holes were required for normal operation. A FET is unipolar in that only one majority current carrier need be considered during normal operation. (holes in P-material channels, and electrons in N-material channels). The FET has three terminals which roughly correspond to the three terminals in a bipolar transistor. The terminals of a FET are called: gate, source, and drain. Fig. 1 shows the relationship of these terminals with one another in a FET, and compares the FET to a bipolar transistor (schematically).

Another major difference between the unipolar and bipolar device, is that the gate of the junction field effect transistor (JFET) is reversed biased (thus the high input resistance), whereas, the bipolar device's base is forward biased for normal operation.

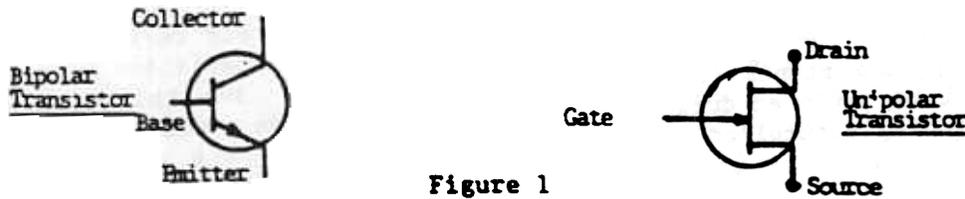


Figure 1
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THE TWO MAJOR TYPES OF FET's:

The two types of FET's are:

1. The junction FET (JFET).
2. The metal oxide semiconductor FET (MOSFET) also called the insulated gate FET (IGFET).

Both types are further classified according to channel material, P or N type. Additionally, the JFET has only one mode of operation. This mode is called the depletion mode. MOSFET's may operate in either the depletion or enhancement mode. Each of these modes will be discussed in detail.

JFET CONSTRUCTION:

The basic construction of the N-channel JFET is shown in Fig. 2. The N-channel JFET consists of a small, thin bar of silicon (in some cases germanium may be used). Terminals are attached to the end, and the drain terminal is attached to the other. Between these connections the silicon bar has a certain resistance. The faces of the bar are doped with P type material; the two strips of P material are connected internally. Their external connection is the gate. A P-channel JFET is of the same basic construction but with a P material bar and N material impurities. Only the N-channel JFET will be discussed during this lesson.

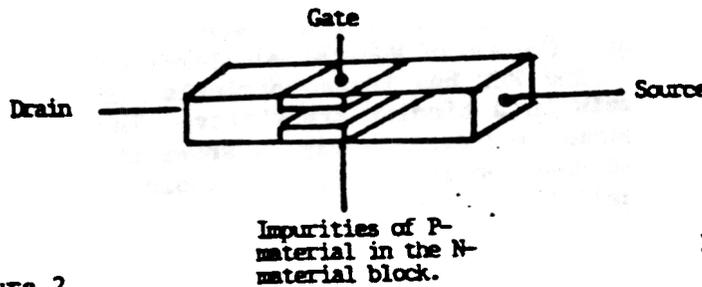


Figure 2
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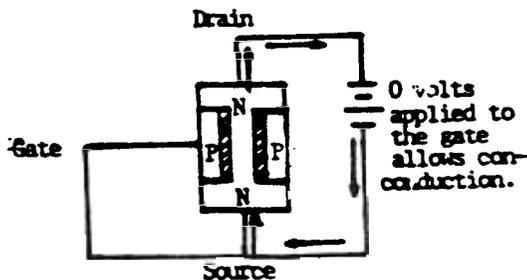
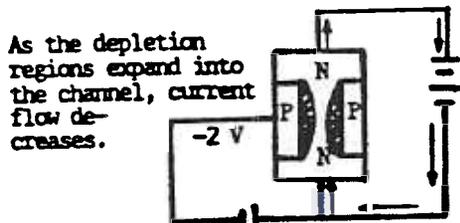


Figure 3
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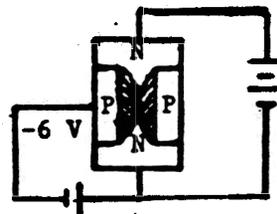
The name field effect refers to the depletion region formed around a PN junction. This depletion region forms an electric field. The current from source to drain must flow through a narrow channel formed between depletion regions. With zero volts applied to the gate, the normal depletion region formed by the PN junction does not penetrate deeply enough into the N-material channel to seriously impede current flow. The channel resistance for zero gate voltage is determined by the doping level of the silicon bar. This resistance and the applied voltage determines the maximum current that will flow through the device. Fig. 3 represents the current flow and the depletion region (the shaded area) of a JFET with zero volts applied to the gate.

As a negative voltage is applied, the gate-source PN junction is reversed biased and the depletion region increases. Recall, the depletion region is composed of ions, not current carriers. This reduction or absence of current carriers forms an increased resistance to current flow. Note that in Fig. 4 the shaded areas representing the depletion regions are penetrating deeper into the channel.



As the depletion regions expand into the channel, current flow decreases.

Figure 4
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When the depletion regions touch, no current flows.

Figure 5
ET10AL-S05

As the negative voltage at the gate increases, the gate-source PN junction is further reversed biased and the depletion region expands yet more deeply into the channel. This reduction in the cross sectional width of the channel reduces current flow through the device, hence reducing drain current. It is possible to cause the gate voltage to become sufficiently negative to completely inhibit current flow through the JFET. The voltage at which this occurs is the gate-source cutoff voltage. The cutoff voltage varies as to the type of FET. Fig. 5 shows the result when gate-source cutoff voltage is applied to the gate. Note that the narrow channel has been totally constricted by the depletion regions.

Because the gate-source junction is normally reversed biased, there is no current flow from source to gate. This results in the desirable high input impedance which is the outstanding advantage of the unipolar device over the bipolar. Typical input impedance for the JFET runs around 100 M .

Unlike the bipolar transistor which is current controlled, the unipolar transistor is voltage controlled. Ideally, voltage at the gate and nothing else controls the amount of current flowing from source to drain.

For optimum operation, the JFET must have either zero volts applied to the gate or some negative voltage (for an N-channel). Should the gate voltage become positive enough to forward bias the gate-source junction damage to the transistor could result. This is because the depletion region is so greatly reduced that the current through the device will greatly increase. At the very least, the high input impedance advantage would be nullified.

JFET SCHEMATIC SYMBOLS:

A JFET is described as being either symmetrical or asymmetrical (or non-symmetrical).

1. Symmetrical refers to the fact that the source and drain can be interchanged in a circuit without adversely affecting the desired operation.
2. Asymmetrical means that the drain and the source are so labeled on the FET. Care must, therefore, be exercised when replacing this type of FET as an improper connection will cause the circuit to malfunction. Most FET's encountered in consumer products are asymmetrical.

Below are illustrated the schematic symbols for the N-channel JFET. Fig. 6 also demonstrates the common abbreviations for the drain, source, and gate. Fig. 7 compares the schematic symbols of the N-channel and the P-channel JFET. Fig. 8 shows the symbol for the asymmetrical JFET. Note that the gate is positioned nearer the source than in the symmetrical JFET.

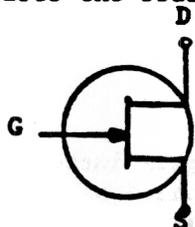


Figure 6 ET10AL-S06

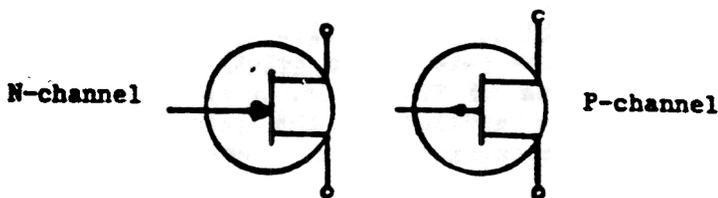


Figure 7 ET10AL-S06

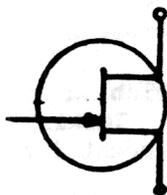


Figure 8 ET10AL-S06

MOSFET CHARACTERISTICS AND CONSTRUCTION:

The second main category of FET's is: the metal oxide semiconductor FET, or MOSFET. The principle characteristics of this unipolar device are as follows:

1. The gate voltage controls the drain current and the input impedance is a very high resistance.
2. The most significant difference between the JFET and the MOSFET is that a positive voltage can be applied to the gate of the MOSFET with zero gate to source current flow. This is due to the fact that the gate and the source does not form a PN junction as the gate is insulated from the silicon bar. With nothing to forward bias, the input impedance remains high even with a positive voltage at the gate.
3. MOSFET's may operate in one of two modes:
 - a. depletion mode
 - b. enhancement mode

Fig. 9(a) shows a silicon bar with drain and source terminals. Fig. 9(b) shows the addition of the substrate to form a narrow channel through which electrons must flow from source to drain. In 9(c), an insulating material is bonded to the silicon bar, and, finally, 9(d) illustrates the metallic gate bonded to the insulation. The MOSFET is also known as the insulated gate FET or IGFET.

MOSFET OPERATION IN THE DEPLETION MODE:

The drain is connected to the positive voltage source V_{DD} (refer to Fig. 10).

The source is connected to a negative terminal of the battery and the substrate is connected to the source to ensure that the PN junction formed by the substrate and the silicon bar does not forward bias. With no voltage at the gate, current flows from source to drain just as it does in the JFET. As a negative voltage is applied to the gate, current carriers within the channel are depleted and current flow is decreased.

To further illustrate the operation, the gate and the N type material of the channel can be viewed as the two plates of a capacitor. The insulating material, then, is the dielectric material between the plates. As a negative going voltage is applied to the gate, a negative charge is developed at the gate. The other plate (the N material of the channel) develops a positive charge. This positive charge forms a depletion region in the channel, narrowing the channel and restricting the current flow.

The more negative the gate voltage becomes, the wider the depletion region becomes and the less current flows. With a sufficiently high negative voltage applied to the gate, the current will cease to flow and cutoff will have been achieved. Thus, the MOSFET acts much like the JFET in the depletion mode.

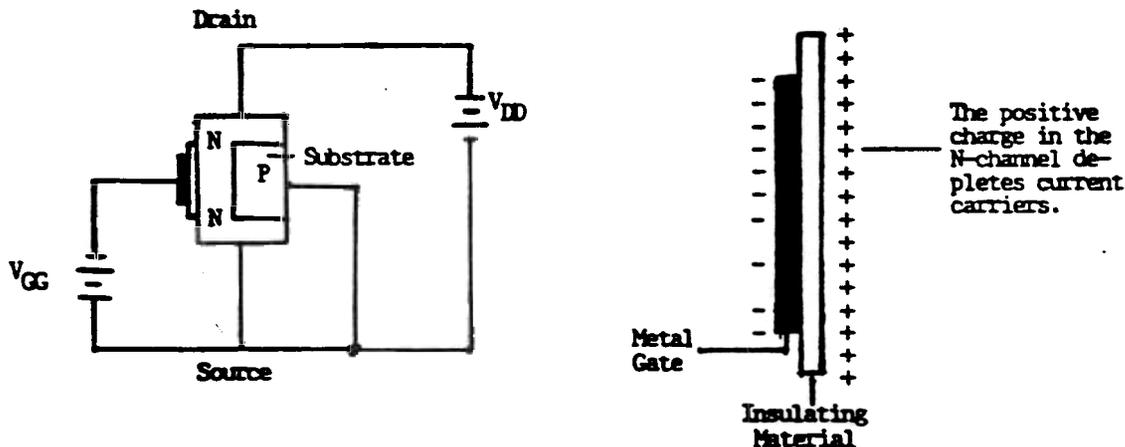


Figure 10 ET10AL-S09

MOSFET OPERATION IN THE ENHANCEMENT MODE:

Since the gate of the MOSFET is insulated and no PN junction formed, a positive voltage may be applied to the gate and the device may be operated in the enhancement mode. Refer to Fig. 11 for the enhancement mode of operation. With a positive voltage applied to the gate, a capacitive effect is induced. This time, however, the positive at the gate produces

a negative charge in the channel which effectively increases the current carriers within the channel. This allows the current in the channel to increase, and electron flow from source to drain has been enhanced. The degree of enhancement is determined by the magnitude of the positive voltage. The resistance, as previously noted, remains high in either mode, ranging in value from about 10,000 M Ω to over 10,000,000 M Ω .

The device shown in Fig. 10 and Fig. 11 is a N channel MOSFET. The P channel MOSFET operates in the same manner except that the applied voltage must be negative. No detailed explanation of a P channel MOSFET will be included in this lesson. Since a channel exists when zero voltage is applied to the gate, this device may be called a normally on MOSFET.

Recall that the a capacitor (on the order of 10 pF) is formed by the gate insulator, and the channel. This produces a built in structural weakness within the MOSFET. Because the insulating material is thin, it can be damaged by static electricity. For protection of this unit, manufacturers provide the leads of the device shorted together. This shorting device should not be removed until the MOSFET is to be placed in the circuit.

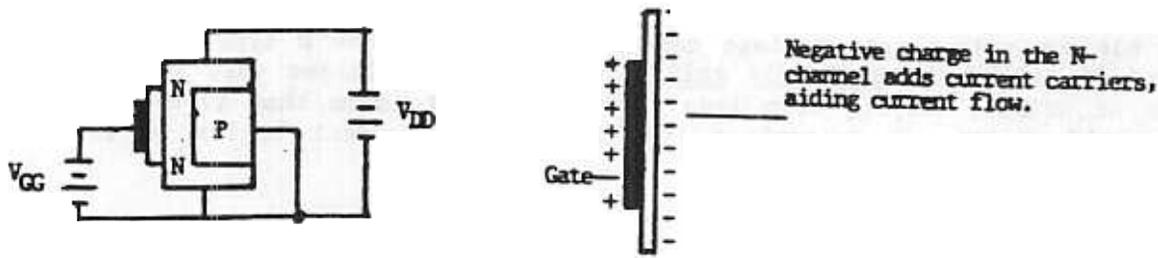


Figure 11
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MOSFET SCHEMATIC SYMBOL:

The block diagram for the MOSFET has been used to better illustrate the device's operation. Like the JFET, the MOSFET also has a schematic representation (see Fig. 12). The schematic for the normally on MOSFET shows an inwardly pointing arrow indicating an N channel. In a MOSFET with a P channel, the arrow points away from the channel.

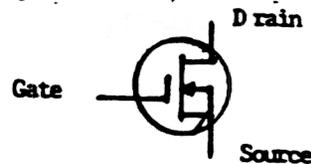


Figure 12 ET10AL-S12

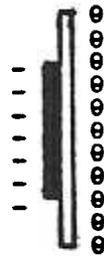
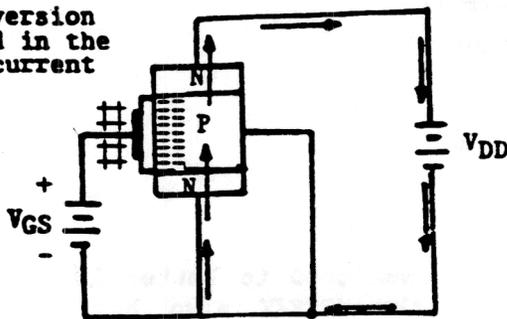
THE ENHANCEMENT ONLY MOSFET:

The enhancement only MOSFET, as the name implies, operates in the enhancement mode only. This type of FET is often found in digital and in switching circuits. Fig. 13 shows a block diagram of the enhancement only MOSFET. Note that the substrate completely divides the silicon bar and no channel exists. Thus, when the gate voltage is zero, the voltage source attempts to force electrons from source to drain, but the P material substrate has only a few thermally produced electrons. Aside from these minority carriers and some surface leakage, the current between source and drain is close to zero. For this reason, the enhancement only MOSFET is also called normally off.

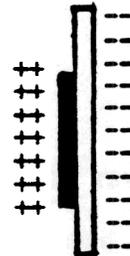
To induce current flow, a positive voltage must be applied to the gate. The gate, insulator, and the P material substrate forms a capacitor. For lower gate voltages the positive charge on the gate induces negative ion formation produced by valence electrons filling holes in the substrate. As the positive potential at the gate is further increased, electrons are placed in orbit around these negative ions. With the gate voltage positive enough, a thin layer of electrons stretch all the way from source to drain through the P material substrate, forming a N channel. The electrons forming this bridge across the P material substrate is called the N type inversion layer.

The minimum gate-source voltage necessary to create the N type inversion layer is called the threshold voltage. Threshold voltages vary with the type of MOSFET, varying from less than one volt to more than five volts. Threshold voltage is determined from the moment current begins to flow through the MOSFET.

With the inversion layer formed in the P-channel, current will flow.



Creating negative ions.



Creating the N-type inversion layer.

Figure 13
ET10AL-S11

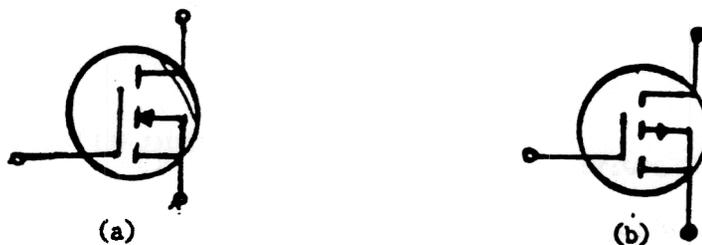


Figure 14
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ENHANCEMENT ONLY MOSFET SCHEMATIC SYMBOL:

When the gate voltage is zero, the enhancement only MOSFET is off as no channel exists for the electrons to flow between the source and the drain. The schematic symbols in Fig's. 14 (a) and (b) have broken lines representing the unformed channel. As already discussed, the threshold voltage creates the N type inversion layer connecting source and drain. The arrow points in when this inversion layer is negative and out when it is positive.

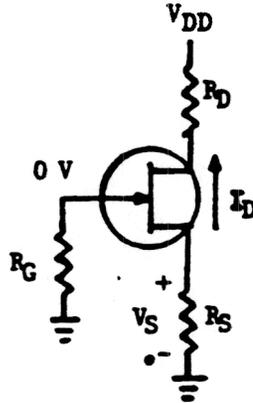


Figure 15 ET10AL-S13

THE JFET AMPLIFIER CIRCUIT:

PC card 49 operates utilizing the concept of source or self biasing. This type of biasing ensures that the gate-source PN junction remains reversed biased for small signal inputs. To better understand this concept, refer to Fig. 15 and the accompanying formulas.

$$V_{DS} = V_{DD} - I_D(R_D + R_S)$$

$$V_S = I_D R_S$$

$$V_G = 0$$

$$V_{GS} = V_G - V_S = 0 - I_D R_S$$

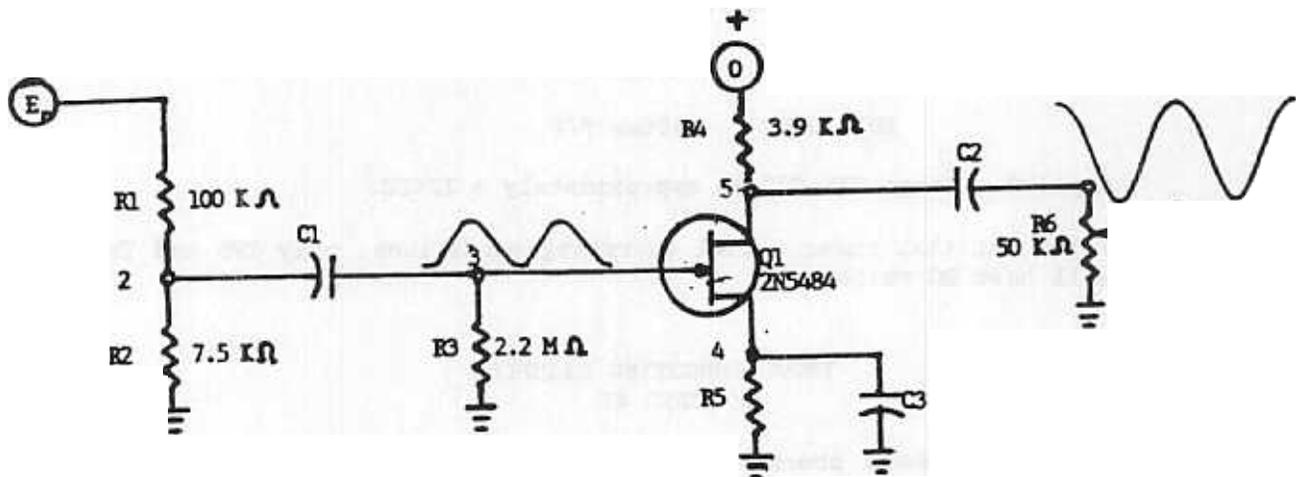
$$V_{GS} = - I_D R_S$$

ET10AL-S13

As is apparent from the formulas, the voltage drop across the source resistor provides the necessary reverse bias to ensure optimum JFET operation. Let us arbitrarily choose a voltage to represent the gate-source bias (-1.5 volts will do) and apply an input voltage of one volt peak to peak. We can see that the input voltage will vary around the bias. Specifically, it will go positive to -1 volt and negative to -2 volts. The gate-source junction, thus, remains reversed biased during all portions of the input signal. This swing in voltage at the gate controls the amount of current through the channel and, hence, changes in the voltage dropped across the load resistor. In this example, the output voltage might vary from 7 volts to 13 volts and the JFET has successfully been made to amplify the 1 volt input.

OPERATION OF PC 49:

PC 49 is an amplification circuit utilizing a JFET which is self biased. Refer to Fig. 16 for the schematic. R5 is the source resistor which will help establish the gate-source bias with 0 volts DC at the gate. R3 is of high resistance to ensure that zero volts is always present at TP 3. This is due to the size of R3 guaranteeing a short time constant prohibiting C1 from developing and holding a charge. R4 is the load resistor and develops the circuit gain. C3 prevents degeneration, and R6 adjusts the amplitude of the output signal. C1 and C2 are coupling capacitors while R1 and R2 form an AC voltage divider. The output waveform for this and all amplifier circuits utilizing FET's is 180 degrees out of phase with the input. This phase shift is characteristic of a unipolar device.



JFET AMP PC 49

Figure 16

ET10AL -S14

Theoretical troubleshooting
CARD 49

1. During the PE, normal voltages/waveforms should be observed and recorded before troubleshooting a faulty circuit.
2. Ensure that proper troubleshooting procedures are followed by each student. Demonstrate correct procedures while showing the troubleshooting examples to the students.
3. The following are examples of voltages normally associated with a correctly functioning card 49. Ensure that the students realize these are approximate voltages only; that actual measurements will differ from circuit to circuit due to variations in applied voltages and component tolerances.

TP2	OVDC	200mv
TP3	OVDC	200mv P/P
	+ .672VDC	0v P/P
	+9.28VDC	1.4v P/P
	OVDC	1.4v P/P
	OVDC	600mv P/P

Applied voltage PIN "0" is approximately + 12VDC.

NOTE: Point out that under normal Operating conditions, only TP5 and TP4 will have DC voltages.

TROUBLESHOOTING EXAMPLES
CARD 49

1.
 - a. Make a waveform check at the circuit output, TP7. Result: No waveform.
 - b. Make a waveform check at the circuit input. TP2 or TP3 may be checked at this time; TP3, however is the preferred choice. Result: TP3 has a normal waveform.
 - c. Make a waveform check at TP5. Result: No waveform.
 - d. Make a DC check at TP5 and TP4. Result TP5 = OVDC, TP4 = OVDC.
 - e. Make PN resistance checks around Q1. Result: Q1 checks out good.
 - f. Because DC voltage decreases below an opening, check resistance across R4. Result: Infinity.
Conclusion: R4 is open.
2.
 - a. Check output waveform, TP7. Result: No waveform.
 - b. Check input waveform, TP3. Result: Waveform normal
 - c. Check TP5. Result: No waveform.

- d. Make DC check, TP5. Result: 2.45VDC.
- e. Make DC check, TP4. Result: 2.45VDC.
- f. Because the same voltage appears at two different points, it may reasonably be concluded that TP5 and TP4 are shorted together.
- g. Check resistance TP5 to TP4. Result: .001 Ω .

Conclusion: Q1 drain and source shorted

3.
 - a. Check output, TP7. Result: No output.
 - b. Check input, TP3. Result: The signal amplitude is greatly decreased.
 - c. Check TP2. Result: Signal amplitude is greatly decreased.
 - d. Check TP5. Result: No waveform.
 - e. Make DC check, TP5. Result: At 2.48VDC, the voltage has decreased.
 - f. Check TP4 DC. Result: At 2.37VDC the voltage has increased.
 - g. Make a check for DC at TP3. Result: TP3 now has DC voltage which is 2.48VDC and therefore equal to the voltage at TP5, leading us to believe the gate-drain might be short.
 - h. Make resistance check TP3 to TP5. Result .001 Ω .

Conclusion: Gate and drain of Q1 is shorted

Analysis: Shorting the gate-drain will forward bias the gate-source PN junction. The PN junction has very little resistance, therefore the presence of bypass capacitor C3 is now felt on the gate terminal which bypasses most of the input signal to ground. The small resistance remaining in the forward biased PN junction develops the small signal seen at TP2 and TP3.

SUMMARY:

The Junction Field Transistor (JFET) is constructed as P-channel or N-channel. The three elements of the JFET are referred to as source, drain, and gate. Current always flows from source to drain. JFET's are made to operate only in the depletion mode, which requires a DC voltage to keep the gate-source PN junction reversed biased.

MOSFET's or IGFET's are also distinguished by the high input impedance and low noise level. MOSFET's can be P-channel or N-channel; MOSFET's may operate in either the depletion mode or the enhancement mode. If operation is in the depletion mode, a gate voltage must be applied to reduce current flow through the channel. If the MOSFET is operating in the enhancement mode, a voltage must be applied to the gate to increase the current flow. Also discussed was the enhancement-only MOSFET, called the normally-off MOSFET. In this type of FET a voltage must be applied to the gate to form a channel which will enable current flow.

All FET's are unipolar devices which means that only one type of majority current carrier is considered during normal operation. The FET combines the high input impedance of the vacuum tube with all the advantages of the transistor.